AMENDMENTS TO THE CLAIMS

Please cancel claims 1-12 without prejudice or disclaimer.

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

13. (Currently Amended) A digital to analog converter circuit ~~according to claim 1~~, comprising:

a plurality of digital to analog converters whose outputs form different but simultaneous portions of an output of said digital to analog converter circuit; and

a distribution circuit for distributing digital input values of said digital to analog converter circuit to said plurality of D/A converters such that, in the case of a continuous incrementing or decrementing of said input values, the individual input values of the plurality of digital to analog converters are incremented or decremented in turn, ~~wherein~~ said distribution circuit ~~comprises~~comprising a divide-by-n counter responsive to said input values of said converter circuit to provide n counter outputs, and n further counters each responsive to a respective one of said n counter outputs, an output from each of said n counters being coupled to a respective one of said plurality of D/A converters.

14. (Currently Amended) A digital to analog converter circuit, comprising:

a plurality of digital to analog converters whose outputs collectively form an output ~~form an output~~ of said digital to analog converter circuit; and

a distribution circuit for distributing digital input values of said digital to analog converter circuit to said plurality of D/A converters such that, in the case of a continuous incrementing of said input values by a given increment amount, the individual input values of the plurality of digital to analog converters are incremented in turn by said given increment amount.

15. (Previously Presented) A digital to analog converter circuit according to claim 14, wherein said distribution circuit comprises a divide-by-n counter responsive to said input values of said converter circuit to provide n counter outputs, and n further counters each responsive to a respective one of said n counter outputs, an output from each of said n counters being coupled to a respective one of said plurality of D/A converters.